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ENERGY RECOVERING APPARATUS AND METHOD FOR PLASMA DISPLAY PANEL

BACKGROUND OF THE INVENTION

Field of the Invention

This invention relates to an energy recovering apparatus and method for a plasma display panel, and more particularly to an energy recovering apparatus and method for a plasma display panel wherein a charge time of the plasma display panel can be shortened with the aid of a compulsory resonance to thereby improve a discharge characteristic.

Description of the Related Art

Recently, there has been developed various flat panel devices that are capable of reducing a heavy weight and a large bulk, which are drawbacks of the cathode ray tube (CRT). Such flat panel display devices include a liquid crystal display (LCD), a field emission display (FED), a plasma display panel (PDP) and an electro-luminescence display (ELD), etc.

The PDP of these flat panel display devices is a display device using a gas discharge, and has an advantage in that it is easy to manufacture a large-dimension panel. The PDP typically includes a three-electrode, alternating current (AC) surface discharge PDP that has three electrodes and is driven with an AC voltage as shown in Fig. 1.

Referring to Fig. 1, a discharge cell of the conventional three-electrode, AC surface-discharge PDP includes a first electrode 12Y and a second electrode 12Z provided on an upper substrate 10, and an address electrode 20X provided on a lower substrate 18.

On the upper substrate 10 provided with the first electrode 12Y and the second electrode 12Z in parallel, an upper dielectric layer 14 and a protective film 16 are disposed. Wall charges generated upon plasma discharge are accumulated into the upper dielectric layer 14. The protective film 16 prevents a damage of the upper dielectric layer 14 caused by a sputtering during the plasma discharge and improves the emission efficiency of secondary electrons. This protective film 16 is usually made from magnesium oxide (MgO).

A lower dielectric layer 22 and barrier ribs 24 are formed on the lower substrate 18 provided with the address electrode 20X. The surfaces of the lower dielectric layer 22 and the barrier ribs 24 are coated with a fluorescent material 26. The address electrode 20X is formed in a direction crossing the first electrode 12Y and the second electrode 12Z. The barrier rib 24 is formed in parallel to the address electrode 20X to prevent an ultraviolet ray and a visible light generated by a discharge from being leaked to the adjacent discharge cells. The phosphorous material 26 is excited by an ultraviolet ray generated during the plasma discharge to generate any one of red, green and blue visible light rays. An inactive gas for a gas discharge is injected into a discharge space defined

between the upper and lower substrate 10 and 18 and the barrier rib 24.

Such a three-electrode, AC surface discharge PDP is driven with being separated into a number of sub-fields. In each sub-field interval, a light emission having a frequency proportional to a weighting value of a video data is conducted to provide a gray scale display. The sub-field is again divided into an initialization period, an address period, a sustain period and an erasure period.

Herein, the initialization period is a period for forming uniform wall charges on the discharge cell. The address period is a period for generating a selective address discharge in accordance with a logical value of the video data. The sustain period is a period for allowing a discharge cell in which the address discharge has been generated to sustain a discharge. The erasure period is a period for erasing a sustain discharge generated in the sustain period.

The address discharge and the sustain discharge of the AC surface-discharge PDP driven in the above manner requires a high voltage more than hundreds of volts. Accordingly, an energy recovering apparatus is used for the purpose of minimizing a driving power required for the address discharge and the sustain discharge. The energy recovering apparatus recovers a voltage between the first electrode 12Y and the second electrode 12Z, to thereby use the recovered voltage as a driving voltage upon the next discharge.

Referring to Fig. 2, energy recovering apparatus 30 and 32 of the PDP having been suggested by U.S. Patent No. 5,081,400 of Weber are symmetrically arranged with respect to each other with having a panel capacitor Cp therebetween. The panel capacitor Cp is an equivalent expression of a capacitance formed between the first electrode Y and the second electrode Y. The first energy recovering apparatus 30 applies a sustain pulse to the first electrode Y. The second energy recovering apparatus 32 operates alternately with respect to the first energy recovering apparatus 30 to thereby apply a sustain pulse to the second electrode Z.

Hereinafter, configurations of conventional energy recovering apparatus of the PDP will be described with reference to the first energy recovering apparatus 30.

The first energy recovering apparatus 30 includes an inductor L connected between a panel capacitor Cp and a source capacitor Cs, first and third switches S1 and S3 connected, in parallel, between the source capacitor Cs and the inductor L, and second and fourth switches S2 and S4 connected, in parallel, between the panel capacitor Cp and the inductor L.

The second switch S2 is connected to a sustain voltage source VS while the fourth switch S4 is connected to a ground voltage source GND. The first to fourth switches S1 to S4 control a current flow.

The source capacitor Cs recovers and charges a voltage charged in the panel capacitor Cp upon sustain discharge

and re-supply the charged voltage to the panel capacitor Cp. The source capacitor Cs is charged with a voltage Vs/2 equal to a half value of the sustain voltage source Vs.

The inductor L forms a natural resonance circuit along with the panel capacitor Cp. At this time, the conventional energy recovering apparatus allows a step of storing energy into the inductor L to overlap with a step of supplying the panel capacitor Cp with the energy stored in the inductor L.

Meanwhile, fifth and sixth diodes D5 and D6 provided between the first and second switches S1 and S2 and the inductor L, respectively prevent a current from flowing in a backward direction.

Fig. 3 is a timing diagram and a waveform diagram representing an on/off timing of switches in the first energy recovering apparatus and an output waveform of the panel capacitor.

An operation procedure of the energy recovering apparatus will be described assuming that 0 volt has been charged in the panel capacitor Cp and a Vs/2 voltage has been charged in the source capacitor Cs prior to a T1 interval.

In a T1 interval, the first switch S1 is turned on, to thereby form a current path extending from the source capacitor Cs, via the first switch S1, the inductor L, into the panel capacitor Cp. If the current path is formed, then a Vs/2 voltage charged in the source capacitor Cs is applied to the panel capacitor Cp. At this time, a Vs

voltage equal to twice the voltage of the source capacitor Cs is charged in the panel capacitor Cp because the inductor L and the panel capacitor Cs form a serial resonance circuit.

In a T2 interval, the second switch S2 is turned on. If the second switch S2 is turned on, then a voltage of the sustain voltage source Vs is applied to the first electrode Y. The voltage of the sustain voltage source Vs applied to the first electrode Y prevents a voltage Vcp of the panel capacitor Cp from falling into less than the sustain voltage source Vs to thereby cause a normal sustain discharge. Meanwhile, since the voltage Vcp of the panel capacitor Cp has risen into Vs in the T1 interval, a driving power supplied from the exterior for the purposing of causing the sustain discharge is minimized.

In a T3 interval, the first switch S1 is turned off. At this time, the first electrode Y sustains a voltage of the sustain voltage source Vs during the T3 interval. In a T4 interval, the second switch S2 is turned off while the third switch S3 is turned off. If the third switch S3 is turned off, then a current path extending from the panel capacitor Cp, via the inductor L and the third switch S3, into the source capacitor Cs is formed to recover a voltage Vcp charged in the panel capacitor Cp into the source capacitor Cs. At this time, a Vs/2 voltage is charged in the source capacitor Cs.

In a T5 interval, the third switch S3 is turned while the fourth switch S4 is turned on. If the fourth switch S4 is turned on, then a current path between the panel capacitor

Cp and the ground voltage source GND is formed, thereby allowing the voltage Vcp of the panel capacitor Cp to 0 volt. In a T6 interval, the T5 state is maintained during a certain time. In real, an alternating current driving pulse supplied to the first electrode Y and the second electrode Z allows the T1 to T6 intervals to be obtained with repeating periodically.

In the mean time, the second energy recovering apparatus 32 operates alternately with respect to the first energy recovering apparatus 30. Accordingly, a sustain pulse voltage Vs having a mutually contrary polarity is applied to the panel capacitor Cp. The sustain pulse voltage Vs having a mutually contrary polarity is applied to the panel capacitor Cp is applied, so that a sustain discharge can be generated from the discharge cells.

However, such conventional energy recovering apparatus 30 and 32 have a problem in that the first energy recovering apparatus 30 provided at the first electrode (Y) side and the second energy recovering apparatus 32 provided at the second electrode (Z) side operate individually to require many circuit elements such as a switching device, etc., and thus to raise a manufacturing cost. Furthermore, a lot of power consumption is caused by a conduction loss of a plurality of switches, such as a diode, a switch device and an inductor, etc., on the current path.

SUMMARY OF THE INVENTION

Accordingly, it is an object of the present invention to provide an energy recovering apparatus and method for a

plasma display panel wherein a charge time of the plasma display panel can be shortened with the aid of a compulsory resonance to thereby improve a discharge characteristic.

In order to achieve these and other objects of the invention, an energy recovering apparatus of a plasma display panel according to one aspect of the present invention includes a first path for charging an inductor using energy from a source capacitor; and a second path, being separated from the source capacitor, for supplying energy of the inductor to the plasma display panel.

The energy recovering apparatus further includes a third path for charging a voltage from a sustain voltage source into the panel; a fourth path for recovering energy charged in the panel to charge the recovered energy, via the inductor, into the source capacitor; and a fifth path for charging a voltage from a ground voltage source into the panel.

Herein, the first path includes a first switching device connected between a second terminal of the source capacitor connected to a ground voltage source and a first terminal of the inductor; and a second switching device connected between a second terminal of the inductor and the ground voltage source.

The first and second switching devices keep a turned-on state during a period when energy from the source capacitor is charged in the inductor through the first path, and shut off the first path in a state in which

energy has been charged in the inductor to thereby derive an inverse voltage into the inductor.

The second path includes a third switching device connected between the second terminal of the inductor and the panel; and a diode connected between a node positioned between the first terminal of the inductor and the first switching device and the ground voltage source to form a path for applying energy from the inductor to the panel.

The third switching device is turned on when the first and second switching devices are turned off, to thereby apply said inverse voltage derived into the inductor to the panel.

The third path includes a fourth switching device connected between the sustain voltage source and the panel.

The fourth path includes the first switching device and the third switching device.

Each of the second and fourth paths further includes a fifth switching device connected between the inductor and the third switching device.

Each of the first to third switching device is connected, in parallel, with a first diode having a first bias direction, and the fifth switching device is connected, in parallel, with a second diode having a second direction which is contrary to the first bias direction.

The fifth switching device becomes a turned-off at the

second path while it becomes a turned-on state at the fourth path.

An energy recovering method for a plasma display panel according to another aspect of the present invention includes the steps of (A) charging energy from a source capacitor into an inductor using a first path including the source capacitor and the inductor; and (B) applying energy of the inductor to the panel using a second path which is separated from the source capacitor and includes the inductor and the plasma display panel.

The energy recovering method further includes the steps of (C) charging a voltage from a sustain voltage source into the panel using a third path including the sustain voltage source and the panel; (D) recovering energy charged in the panel to charge the recovered energy into the source capacitor using a fourth path including the panel, the inductor and the source capacitor; and (E) charging a voltage from the ground voltage source into the panel using a fifth path including the ground voltage source and the panel.

Herein, said (A) step includes charging energy from the source capacitor into the inductor through the first path; and shutting off the first path in a state in which energy has been charged in the inductor to thereby derive an inverse voltage into the inductor.

Said (B) step includes charging said inverse voltage derived into the inductor to the panel through the second path.

BRIEF DESCRIPTION OF THE DRAWINGS

These and other objects of the invention will be apparent from the following detailed description of the embodiments of the present invention with reference to the accompanying drawings, in which:

Fig. 1 is a perspective view showing a structure of a conventional three-electrode AC surface-discharge plasma display panel;

Fig. 2 is a circuit diagram of an energy recovering apparatus of the conventional plasma display panel;

Fig. 3 is a timing diagram and a waveform diagram representing an ON/OFF timing of each switch shown in Fig. 2 and an output waveform of the panel capacitor, respectively;

Fig. 4 is a circuit diagram of an energy recovering apparatus of a plasma display panel according to a first embodiment of the present invention;

Fig. 5 is a timing diagram and a waveform diagram representing an ON/OFF timing of each switch shown in Fig. 4 and an output waveform of the panel capacitor, respectively;

Fig. 6 is a circuit diagram showing an ON/OFF state of each switch and a current path in the T1 interval shown in Fig. 5;

Fig. 7 is a circuit diagram showing an ON/OFF state of each switch and a current path in the T2 interval shown in Fig. 5;

Fig. 8 is a circuit diagram showing an ON/OFF state of each switch and a current path in the T3 interval shown in Fig. 5;

Fig. 9 is a circuit diagram showing an ON/OFF state of each switch and a current path in the T4 interval shown in Fig. 5;

Fig. 10 is a circuit diagram showing an ON/OFF state of each switch and a current path in the T5 interval shown in Fig. 5;

Fig. 11 is a circuit diagram of an energy recovering apparatus of a plasma display panel according to a second embodiment of the present invention;

Fig. 12 is a timing diagram and a waveform diagram representing an ON/OFF timing of each switch shown in Fig. 11 and an output waveform of the panel capacitor, respectively;

Fig. 13 is a circuit diagram showing an ON/OFF state of each switch and a current path in the T1 interval shown in Fig. 11;

Fig. 14 is a circuit diagram showing an ON/OFF state of each switch and a current path in the T2 interval shown in Fig. 11;

Fig. 15 is a circuit diagram showing an ON/OFF state of each switch and a current path in the T3 interval shown in Fig. 11;

Fig. 16 is a circuit diagram showing an ON/OFF state of each switch and a current path in the T4 interval shown in Fig. 11; and

Fig. 17 is a circuit diagram showing an ON/OFF state of each switch and a current path in the T5 interval shown in Fig. 11.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

Referring to Fig. 4, there is shown an energy recovering

apparatus of a plasma display panel (PDP) according to the first embodiment of the present invention.

The energy recovering apparatus includes a panel capacitor Cp that is an equivalent capacitance formed between a first electrode Y and a second electrode Z, a source capacitor Cs connected between the panel capacitor Cp and a ground voltage source GND, an inductor L connected between the panel capacitor Cp and the source capacitor Cs, a first switch SW1 connected between the source capacitor Cs and the inductor L, a second switch SW2 connected between a first node N1 positioned between the inductor L and the first electrode Y of the panel capacitor Cp and the ground voltage source GND, a third switch SW3 connected between the first node N1 and the first electrode Y of the panel capacitor Cp, a fourth switch SW4 connected between a second node N2 positioned between the third switch SW3 and the first electrode Y of the panel capacitor Cp and the sustain voltage source Vs, and a diode connected between a third node N3 positioned between the first switch SW1 and the inductor L and the ground voltage source GND.

The sustain voltage source VS generates a sustain voltage VS supplied to the panel capacitor Cp.

The inductor L stores energy from the source capacitor Cs with the aid of a compulsory resonance provided by itself and the source capacitor Cs and thereafter applies the stored energy to the panel capacitor Cp. At this time, energy is not applied to the panel capacitor Cp during a period when energy is stored in the inductor L. As

described above, energy is stored in the inductor L by a compulsory resonance between the inductor L and the source capacitor Cs and thereafter the energy stored in the inductor L is applied to the panel capacitor Cp, so that a sustain pulse has a fast rising slope.

Each of the first to fourth switches SW1 to SW4 controls a flow of current.

The diode D shuts off a backward current from the inductor L and the source capacitor Cs. Further, the diode D forms a path for applying energy from the inductor L to the panel capacitor Cp.

Fig. 5 is a timing diagram and a waveform diagram representing an ON/OFF timing of each switch and a voltage applied to the panel capacitor in the energy recovering apparatus of the PDP according to the first embodiment of the present invention shown in Fig. 4.

An energy recovering apparatus and method according to the first embodiment of the present invention in Fig. 5 will be described in conjunction with Fig. 4.

An operation procedure of the energy recovering apparatus will be described assuming that 0 volt has been charged in the panel capacitor Cp and a certain voltage has been charged in the source capacitor Cs prior to a T1 period.

In the T1 period, the first and second switches SW1 and SW2 are turned on, to thereby form a current path extending from the source capacitor Cs, via the first

switch SW1, the third node N3, the inductor L, the first node N1 and the second switch SW2, into the ground voltage source GND as shown in Fig. 6. Thus, a serial compulsory resonance circuit between the inductor L and the source capacitor Cs are provided. Accordingly, the inductor L stores energy form the source capacitor Cs. At this time, the energy stored in the inductor L is controlled in accordance with switching timings of the first and second switches SW1 and SW2.

In a T2 period, the first and second switches SW1 and SW2 are turned off while the third switch SW3 is turned on. The third switch SW3 is turned on, to thereby form a current path extending from the ground voltage source GND, via the diode D, the third node N3, the inductor L, the first node N1, the third switch SW3, the second node N2 and the panel capacitor Cp, into the ground voltage source GND as shown in Fig. 7. At this time, an inverse voltage is derived into the inductor L at the instant that the first and second switches SW1 and SW2 are turned off, and the derived inverse voltage is applied to the panel capacitor Cp through said current path. Thus, the panel capacitor Cp charges the inverse voltage from the inductor L. At this time, a voltage Vcp of the panel capacitor Cp rises from 0 volt by the inverse voltage from the inductor L at a fast slope.

In a T3 period, the third switch SW3 is turned off while the fourth switch SW4 is turned on. The fourth switch SW4 is turned on, to thereby form a current path extending from the sustain voltage source Vs, via the fourth switch SW4, the second node N2 and the panel capacitor Cp, into

the ground voltage source GND as shown in Fig. 8. Thus, a sustain voltage Vs from the sustain voltage source Vs is supplied to the first electrode Y of the panel capacitor Cp. A voltage of the sustain voltage source Vs supplied to the first electrode Y of the panel capacitor Cp prevents a voltage of the panel capacitor Cp from falling into less than the sustain voltage source Vs, thereby causing a normal sustain discharge.

In a T4 period, the fourth switch SW4 is turned off while the first and third switches SW1 and SW3 are turned on. The first and third switches SW1 and SW3 are turned on, to thereby form a current path extending from the panel capacitor Cp, via the second node N2, the third switch SW3, the first node N1, the inductor L, the third node N3, the first switch SW1 and the source capacitor Cs, into the ground voltage source GND as shown in Fig. 9. Thus, a voltage charged in the panel capacitor Cp is recovered into the source capacitor Cs through said current path.

In a T5 period, the first switch SW1 is turned off while the third switch SW3 is kept at a turned-on state and the second switch SW2 is turned on. Thus, a current path extending from the panel capacitor Cp, via the second node N2, the third switch SW3, the first node N1 and the second switch SW2, into the ground voltage source GND as shown in Fig. 10 is formed. Thus, the panel capacitor Cp falls into a ground voltage GND through said current path.

In a T6 period, the T5 state is kept during a predetermined time. In real, a sustain pulse applied to the panel capacitor Cp is provided with periodically

repeating the T1 to T6 periods.

As described above, the energy recovering apparatus and method of the PDP according to the first embodiment of the present invention stores energy stored in the source capacitor Cp into the inductor L using a compulsory resonance between the source capacitor Cs and the inductor L and applies the stored energy to the panel capacitor Cp. At this time, energy is not applied to the panel capacitor during a period when the energy stored in the source capacitor Cs is being stored in the inductor L. Thus, the energy recovering apparatus and method of the PDP according to the first embodiment of the present invention charges the energy stored in the inductor L into the panel capacitor by a compulsory resonance, so that it can obtain a fast rising slope of the sustain pulse applied to the panel capacitor Cp, thereby reducing a charge time of energy charged in the panel capacitor Cp. Accordingly, it becomes possible to improve a discharge characteristic owing to the fast rising slope of the sustain pulse.

Referring to Fig. 11, there is shown an energy recovering apparatus of a plasma display panel (PDP) according to the second embodiment of the present invention.

The energy recovering apparatus includes a panel capacitor Cp that is an equivalent capacitance formed between a first electrode Y and a second electrode Z, a source capacitor Cs connected between the panel capacitor Cp and a ground voltage source GND, an inductor L connected between the panel capacitor Cp and the source capacitor Cs, a first switching device Q1 connected between the source

capacitor Cs and the inductor L, a second switching device Q2 connected between a first node N1 positioned between the inductor L and the first electrode Y of the panel capacitor Cp and the ground voltage source GND, a third switching device Q3 connected between the first node N1 and the first electrode Y of the panel capacitor Cp, a fourth switching device Q4 connected between a second node N2 positioned between the third switching device Q3 and the first electrode Y of the panel capacitor Cp and the sustain voltage source Vs, a fifth switching device Q5 connected between the third switching device Q3 and the inductor L, and a diode D connected between a third node N3 positioned between the first switching device Q1 and the inductor L and the ground voltage source GND.

The sustain voltage source VS generates a sustain voltage VS supplied to the panel capacitor Cp.

The inductor L stores energy from the source capacitor Cs with the aid of a compulsory resonance provided by itself and the source capacitor Cs and thereafter applies the stored energy to the panel capacitor Cp. At this time, energy is not applied to the panel capacitor Cp during a period when energy is stored in the inductor L. As described above, energy is stored in the inductor L by a compulsory resonance between the inductor L and the source capacitor Cs and thereafter the energy stored in the inductor L is applied to the panel capacitor Cp, so that a sustain pulse has a fast rising slope.

Each of the first to fifth switching devices Q1 to Q5 controls a flow of current. Such first to fifth switching

devices Q1 to Q5 are connected, in parallel, to first to fifth diodes, respectively. The first to fifth diodes can be used as internal diodes of the first to fifth switching devices Q1 to Q5. Alternatively, the first to fifth diodes may be used as external diodes thereof. Meanwhile, each of the first to fifth switching devices Q1 to Q5 employs any one of semiconductor switching devices such as a metal oxide semiconductor field-effect transistor (MOSFET), an insulated gate bipolar transistor (IGBT), a silicon-controlled rectifier (SCR), a bipolar junction transistor (BJT) and a high electron mobility transistor (HEMT), etc.

The diode D shuts off a backward current from the inductor L and the source capacitor Cs. Further, the diode D forms a path for applying energy from the inductor L to the panel capacitor Cp.

Fig. 12 is a timing diagram and a waveform diagram representing an ON/OFF timing of each switch and a voltage applied to the panel capacitor in the energy recovering apparatus of the PDP according to the second embodiment of the present invention shown in Fig. 11.

An energy recovering apparatus and method according to the first embodiment of the present invention in Fig. 12 will be described in conjunction with Fig. 11.

An operation procedure of the energy recovering apparatus will be described assuming that 0 volt has been charged in the panel capacitor Cp and a certain voltage has been charged in the source capacitor Cs prior to a T1 period.

In the T1 period, the first and second switching devices Q1 and Q2 are turned on, to thereby form a current path extending from the source capacitor Cs, via the first switching device Q1, the third node N3, the inductor L, the first node N1 and the second switching device Q2, into the ground voltage source GND as shown in Fig. 13. Thus, a serial compulsory resonance circuit between the inductor L and the source capacitor Cs are provided. Accordingly, the inductor L stores energy form the source capacitor Cs. At this time, the energy stored in the inductor L is controlled in accordance with switching timings of the first and second switching devices Q1 and Q2.

In a T2 period, the first and second switching devices Q1 and Q2 are turned off while the third switching device Q3 is turned on. The third switching device Q3 is turned on, to thereby form a current path extending from the ground voltage source GND, via the diode D, the third node N3, the inductor L, the first node N1, a diode of the fifth switching device Q5, the third switching device Q3, the second node N2 and the panel capacitor Cp, into the ground voltage source GND as shown in Fig. 14. At this time, an inverse voltage is derived into the inductor L at the instant that the first and second switching devices Q1 and Q2 are turned off, and the derived inverse voltage is applied to the panel capacitor Cp through said current path. Thus, the panel capacitor Cp charges the inverse voltage from the inductor L. At this time, a voltage Vcp of the panel capacitor Cp rises from 0 volt by the inverse voltage from the inductor L at a fast slope.

In a T3 period, the third switching device Q3 is turned

off while the fourth switching device Q4 is turned on. The fourth switching device Q4 is turned on, to thereby form a current path extending from the sustain voltage source Vs, via the fourth switching device Q4, the second node N2 and the panel capacitor Cp, into the ground voltage source GND as shown in Fig. 15. Thus, a sustain voltage Vs from the sustain voltage source Vs is supplied to the first electrode Y of the panel capacitor Cp. A voltage of the sustain voltage source Vs supplied to the first electrode Y of the panel capacitor Cp prevents a voltage of the panel capacitor Cp from falling into less than the sustain voltage source Vs, thereby causing a normal sustain discharge.

In a T4 period, the fourth switching device Q4 is turned off while the fifth switching device Q5 is turned on. The fifth switching device Q5 is turned on, to thereby form a current path extending from the panel capacitor Cp, via the second node N2, a diode of the third switching device Q3, the fifth switching device Q5, the first node N1, the inductor L, the third node N3, a diode of the first switching device Q1 and the source capacitor Cs, into the ground voltage source GND as shown in Fig. 16. Thus, a voltage charged in the panel capacitor Cp is recovered into the source capacitor Cs through said current path.

In a T5 period, the fifth switching device Q5 keeps a turned-on state while the second switching device Q2 is turned on. Thus, a current path extending from the panel capacitor Cp, via the second node N2, a diode of the third switching device Q3, the fifth switching device Q5, the first node N1 and the second switching device Q2, into the

ground voltage source GND as shown in Fig. 17 is formed. Thus, the panel capacitor Cp falls into a ground voltage GND through said current path.

In a T6 period, the T5 state is kept during a predetermined time. In real, a sustain pulse applied to the panel capacitor Cp is provided with periodically repeating the T1 to T6 periods.

As described above, the energy recovering apparatus and method of the PDP according to the second embodiment of the present invention stores energy stored in the source capacitor Cp into the inductor L using a compulsory resonance between the source capacitor Cs and the inductor L and applies the stored energy to the panel capacitor Cp. At this time, energy is not applied to the panel capacitor during a period when the energy stored in the source capacitor Cs is being stored in the inductor L. Thus, the energy recovering apparatus and method of the PDP according to the first embodiment of the present invention charges the energy stored in the inductor L into the panel capacitor by a compulsory resonance, so that it can obtain a fast rising slope of the sustain pulse applied to the panel capacitor Cp, thereby reducing a charge time of energy charged in the panel capacitor Cp. Accordingly, it becomes possible to improve a discharge characteristic owing to the fast rising slope of the sustain pulse.

As described above, the energy recovering apparatus and method of the PDP according to the present invention stores energy stored in the source capacitor into the inductor using a compulsory resonance between the source

capacitor and the inductor and applies the stored energy to the panel capacitor. Thus, the energy recovering apparatus and method of the PDP according to the present invention charges the energy stored in the inductor into the panel capacitor by a compulsory resonance, so that it can obtain a fast rising slope of the sustain pulse applied to the panel capacitor, thereby reducing a charge time of energy charged in the panel capacitor. Accordingly, it becomes possible to improve a discharge characteristic owing to the fast rising slope of the sustain pulse.

Although the present invention has been explained by the embodiments shown in the drawings described above, it should be understood to the ordinary skilled person in the art that the invention is not limited to the embodiments, but rather that various changes or modifications thereof are possible without departing from the spirit of the invention. Accordingly, the scope of the invention shall be determined only by the appended claims and their equivalents.